UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,395	10/30/2003	Rudolf J. Hofmeister	15436.247.11.1	7465

22913 7590 05/09/2007

WORKMAN NYDEGGER
(F/K/A WORKMAN NYDEGGER & SEELEY)
60 EAST SOUTH TEMPLE
1000 EAGLE GATE TOWER
SALT LAKE CITY, UT 84111

EXAMINER	
MALKOWSKI, KENNETH J	
ART UNIT	**PAPER NUMBER**
2613	

MAIL DATE	DELIVERY MODE
05/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,395	HOFMEISTER ET AL.	
	Examiner	Art Unit	
	Kenneth J. Malkowski	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,909,848 to Kim et al. in view of U.S. Patent No. 6,631,144 to Johansen et al. and further in view of U.S. Patent No. 6,956,847 to Heston et al.

With respect to claim 1, Kim discloses an opto-electric device (102, Fig 1 (photo-electric transducers))(column 1 lines 39-48 (photo-electric transducers)), comprising: a circuit having an automatically selectable data rate (column 4 lines 34-40 (bit rate is automatically selected based on temperature information based on a CPU (181, Fig 2) control signal)) and configured to generate a loss of lock signal when an input data stream has a data rate out of range of an operational rate at which the optoelectronic device is set (column 3 lines 20-27 (if bit rate of converted electrical signal (input data stream) is not consistent with pre-set bit rate, each BICDR outputs a loss of lock signal)), the circuit comprising: a data stream input for receiving the input data stream (Fig 1 (inputted optical signals)); and a data rate select input for configured to enable selection and setting of the operational data rate of the circuit (adjust bit rate)(column 4 lines 3-40 (data operational rate is selected by controller (180, Fig 2) which is enabled by comparing an inputted loss of lock signal and a DC level value representing the bit rate of the output signals form the DMUX (110, Fig 2)); and a controller coupled to the data rate select input and

configured to enable automatic adjustment of the operational data rate of the circuit in response to receipt of the loss of lock signal (column 3 lines 20-27 (column 3 lines 20-27 (if bit rate of converted electrical signal (input data stream) is not consistent with pre-set bit rate, each BICDR outputs a loss of lock signal))(column 4 lines 3-12 (said error signal is then sent to CPU (181, Fig 2))(column 4 lines 34-40 (CPU adjusts bit rate in response to said error signal)). However, Kim fails to disclose that said circuitry is implemented as an integrated circuit. Johansen, from the same field of endeavor also discloses multi-rate transponder system including usage of a clock and data recovery (CDR) circuit (column 5 lines 35-40), a phase locked loop (PLL) based CDR circuit (column 6 lines 45-50), and a selectable bit rate (column 5 lines 58-65) all implemented into an integrated circuit (Figures 2 and 3)(column 14 lines 20-27 (integrated receiver/transmitter chip))(column 14 lines 59-63 (integrated circuit)). At the time of invention it would have been obvious to one of ordinary skill in the art to implement the circuitry as disclosed by Kim into an integrated circuitry format as disclosed by Johansen. The motivation for doing so would have been to minimize hardware requirements and improve reliability of network nodes (column 9 lines 21-26) and to take advantage of certain component reductions such as pin count, die area, and signal coupling (column 14 lines 48-55).

Furthermore, Kim in view of Johansen fail to disclose ceasing to adjust the selectable data rate once all selectable data rates have been attempted, whether or not the loss of lock signal has ceased. In applicants specification, applicant further defines the cessation of adjustment of the selectable data rate as in effect bypassing the CDR circuit (applicants specification: Figure 1305, 1406 (bypass, Figure 4))(applicants specification: 1614, Figure 5 (bypass))(applicants specification: page 20 paragraph 54 (CDR is designed to run at 4, 2, or 1 Gb/s or lower, if LOL

persists beyond these rates the CDR determines that the operational data rate is slower than 2 Gb/s and takes itself offiline)).

Heston, from the same field of endeavor discloses an optical network element (204, Figure 2a), which selects from one of several selectable data rates (column 2 lines 29-30 (the present invention relates to a line card with multiple ports and multiple rates))(column 2 lines 55-60 (ports are configured to receive one of an OC-3, OC-12 or OC-48 signal))(column 7 lines 38-42 (clock and data recovery modules include mapping functionality which allows OC-3, OC-12 or OC-48 signals to be mapped to a common signal format)) and includes a controller that ceases to adjust the selectable data rate once all selectable data rates have been attempted (Figure 7 depicts at steps 708 and 712 attempts to adjust the selectable data rates until all selectable data rates, in this case, OC-3, OC-12 or OC-48 signals, have been attempted. Once all have been attempted data rate adjustment ceases)(column 7 lines 39-56 (if the incoming signal is not one of the selectable data rates (OC-3, OC-12 or OC-48 signals), for instance a Gigabit Ethernet signal, the signal bypasses the cdr module 312, in the same manner as the claimed invention)). Therefore, it would have been obvious to implement cessation of selectable data rate adjustment into the transponder system as taught by Kim in view of Johansen. The motivation for doing so would be to maximally utilize recovery circuitry for signals that are most common to telecommunications signaling and allows for use of less complicated and more conventional components (Heston: column 7 lines 48-56 (typical cdr modules allow programmable bandwidth limiting that provides the capacity to deliver OC-3, OC-12 or OC-48 signals and gigabit Ethernet services off the same physical ports which or coupled to optics)).

With respect to claim 2, Kim in view of Johansen and further in view of Heston disclose the opto-electric device as recited in claim 1 (Kim: 102, Fig 1 (photo-electric transducers))(Kim: column 1 lines 39-48 (photo-electric transducers)), wherein the integrated circuit comprises one of: a clock and data recover integrated circuit; a multiplexer/demultiplexer integrated circuit; and, a serializer/deserializer integrated circuit (Johansen: column 6 lines 45-50 (PLL based CDR circuit; integrated circuit design))(Kim: 121, 141 Fig 2 (CDR receivers and transmitters))(Kim: column 3 lines 5-9 (bit rate independent clock and data recovery receivers)(Kim: column 4 lines 56-62 bit rate independent clock and data recovery transmitters)).

With respect to claim 3, Kim in view of Johansen and further in view of Heston disclose the opto-electric device as recited in claim 1, wherein the integrated circuit includes a sub-circuit that provides clock and data recovery for a plurality of data rates (Kim: column 4 lines 38-46 (control signal is sent to bit rate independent clock and data recovery receiver to adjust bit rate))(Johansen: column 2 lines 21-34 a CDR circuit comprised within a multi-rate transponder system), the controller (Kim: 180, Fig 2)(Kim: column 3 lines 32-35 (control device))(Johansen: column 4 lines 26-37 (system controller)) being configured to adjust the selectable data rate to each of the plurality of data rates (Kim: column 4 lines 38-40 (CPU 181 generates a control signal to adjust the bit rate))(Johansen: column 9 lines 7-31 (CDR is adapted to provide a selectable nominal bit rate, selected from a plurality of predetermined bit nominal bit rates, this embodiment allows the controller to perform on-the fly alteration of the current communication protocol supported by the multi-rate transponder circuit)).

With respect to claim 5, Kim in view of Johansen and further in view of Heston disclose the opto-electric device as recited in claim 1 includes the controller (Kim: 180, Fig 2)(Kim:

column 3 lines 32-35 (control device))(Johansen: 200, Fig 1) and the integrated circuit reside together on the same chip (Johansen: 100, 300 Fig 1)(Johansen: column 14 lines 45-55 partitioning between circuit blocks is not limiting for the scope of the invention, circuit blocks can be formed on a common substrate, use common signal coupling and/or common power nets)(Johansen: column 12 lines 54-56).

With respect to claims 7-8, Kim in view of Johansen and further in view of Heston disclose the optoelectric device as recited in claim 1, wherein the device is compatible with Fiber Channel Protocol (Johansen: column 1 lines 59-64 (the chip set and transponder system should be capable of supporting reception/transmission of several differing communication protocols)(Kim: column 1 lines 21-29 (wherein several fiber channel systems are listed which have the capability to be compatible with 2 Gb/s bit rates (up to 2.5 Gb/s)(ie. Ethernet, escon, fddi, and atm))).

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,909,848 to Kim et al. in view of U.S. Patent No. 6,631,144 to Johansen et al. and further in view of U.S. Patent No. 6,956,847 to Heston et al. and further in view of U.S. Patent Application No. 2002/0060824 to Liou et al.

With respect to claim 6, Kim in view of Johansen and further in view of Heston disclose the optoelectric device as recited in claim 1, however Kim in view of Johansen fail to disclose a rate of about 10 Gb/s as such a data rate was not common at the time of filing of the application submitted by Kim, rather, a 2.5 Gb/s data rate is disclosed. Liou, from the same field of endeavor discloses an electro-optic with CDR and control module (Fig 1). Liou teaches said module wherein the first serial electrical data stream had a data rate of 10 Gb/s or faster (page 3

paragraph 24)(page 1 paragraph 6). At the time of invention it would have been obvious to one skilled in the art to replace the older laser transmission technology associated with the transponder as taught by Kim in view of Johansen with the electro-absorption modulated FP laser as taught by Liou. The motivation for doing so would have been to achieve a data stream rate of 10 Gb/s and to achieve a superior transmission characteristic exemplified by the eye diagram model (Liou: Page 1 paragraph 6)(Liou: page 3 paragraph 24).

4. Claims 9-10 and 12-13 (formerly claims 13-15) and 16 (formerly claim 17) are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,631,144 to Johansen et al. in view of U.S. Patent Application Publication No. 2002/0021468 to Kato et al.

With respect to claims 9 and 12-13, Johansen discloses a signal modification integrated circuit (Figures 2 and 3)(column 14 lines 20-27 (integrated receiver/transmitter chip))(column 14 lines 59-63 (integrated circuit)) suitable for use in connection with an opto-electric device (column 1 lines 11-15 (interconnects high-speed optical network applications and standard system controllers)), the signal modification integrated circuit comprising: a receive circuit configured to operate at any one of a plurality of automatically selectable data rates (column 1 lines 59-64)(column 9 lines 21-29 (on the fly alteration of the current communication protocol)(column 17 lines 42-50 control the timing frequency of the CDR circuit for a higher or lower bit rate than the nominal rate) and further configured to generate a loss of lock signal when a data stream associated with the receive circuit has a data rate out of range of an operational data rate at which the opto-electric device is set (column 12 lines 16-46 (loop selection means comprises a lock detection circuit to compare the reference clock signal with the line clock signal. If these frequencies differ with an amount larger than the threshold the incoming data

stream is considered lost and as a result the bit rate altered)), and the transmit circuit being configured to set the operational data rate of the opto-electric device to successive data rates (column 17 lines 43-50 (nominal bit rate of 2.5 Gb/s can be controlled to be a higher or lower bit rate) included in the plurality of automatically selectable data rates until the loss of lock signal asserted by the receive circuit ceases ((columns 17-18 lines 63-67 and 1-12 (lock detect circuit continuously monitors incoming line clock signal wherein only if there is a loss of lock brought on by a frequency difference larger than a predetermined value will a change in bit rate occur (scaling of PLL); therefore, if the loss of lock signal ceases the selection or scaling of successive data rates also subsides)(column 16 lines 6-19 (scaling of PLL effects output transmission bit rate of serial data by changing ratio values Y and X)). However, Johansen fails to disclose a functionally identical transmit circuit on the same integrated circuit as said receive circuit. Kato, from the same field of endeavor discloses an optical communication module (10, Fig 3) wherein the module contains both a signal reception process (110, Fig 3) and a signal transmission process (120, Fig 3) formed on a single integrated circuit semiconductor chip (abstract). At the time of invention, it would have been obvious to one of ordinary skill in the art to substantially duplicate the receive circuitry as taught by Johansen to create a transmit circuitry substantially similar to said receiver circuitry formed on a single integrated circuit semiconductor chip as taught by Kato. The motivation for having a pair of transmit/receive circuits would have been to create a bidirectional transponder module as opposed to a unidirectional transponder module. Also, having a module as taught by Kato allows for a loop-back path provided between the transmission IC and the reception IC to test for a correlation between input and output signals (Kato: page 1 paragraph 9). With further reference to claims 13 and 14, Johansen in view of Kato

teach that the receiver having de-multiplexer (Johansen: column 3 lines 62-67 (receiver portion may comprise a de-multiplexer))(Kato: 131, Fig 2) and the transmitter having a multiplexer (Johansen: column 4 lines 1-6 (transmitting portion may comprise a multiplexer))(Kato: 151, Fig 2).

With respect to claim 10, Johansen in view of Kato disclose the signal modification integrated circuit as recited in claim 9, wherein the signal modification integrated circuit comprises a clock data recover integrated circuit that includes an oscillator serving as a reference clock (Johansen: column 17 lines 14-20.(VCO generates a reference clock signal)(415, 70 Fig 1).

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,631,144 to Johansen et al. in view of U.S. Patent Application Publication No. 2002/0021468 to Kato et al. and further in view of U.S. Patent Application No. 2002/0060824 to Liou et al.

With respect to claim 11 Johansen in view of Kato disclose the signal modification integrated circuit as recited in claim 9, however, Johansen in view of Kato fail to disclose a rate of about 4 Gb/s, rather, a 2.5 Gb/s data rate and below is disclosed. Liou, from the same field of endeavor discloses an electro-optic with CDR and control module (Fig 1). Liou teaches said module wherein the first serial electrical data stream had a data rate of 10 Gb/s or faster (page 3 paragraph 24)(page 1 paragraph 6). At the time of invention it would have been obvious to one skilled in the art to replace the transmission technology associated with the transponder as taught by Johansen in view of Kato with the electro-absorption modulated FP laser as taught by Liou. The motivation for doing so would have been to achieve a superior transmission characteristic

exemplified by the eye diagram model and thereby achieving a data stream rate of up to 10 Gb/s including aforementioned 4 Gb/s (Liou: Page 1 paragraph 6)(Liou: page 3 paragraph 24).

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,631,144 to Johansen et al. in view of U.S. Patent Application Publication No. 2002/0021468 to Kato et al. and further in view of U.S. Patent No. U.S. Patent No. 6,956,847 to Heston et al.

With respect to claims 14, Johansen discloses a method for automatically selecting and setting an operational data rate of an optoelectronic device (title (multi-rate tranponder system)), the method comprising: receiving an input data stream having an input data rate (10, Figure 1 (line rate = K)); generating a loss of lock signal when a data stream associated with the receive circuit has a data rate out of range of an operational data rate at which the opto-electric device is set (column 12 lines 16-46 (loop selection means comprises a lock detection circuit to compare the reference clock signal with the line clock signal. If these frequencies differ with an amount larger than the threshold the incoming data stream is considered lost and as a result the bit rate altered)), and the transmit circuit being configured to set the operational data rate of the opto-electric device to successive data rates (column 17 lines 43-50 (nominal bit rate of 2.5 Gb/s can be controlled to be a higher or lower bit rate) included in the plurality of automatically selectable data rates until the loss of lock signal asserted by the receive circuit ceases ((columns 17-18 lines 63-67 and 1-12 (lock detect circuit continuously monitors incoming line clock signal wherein only if there is a loss of lock brought on by a frequency difference larger than a predetermined value will a change in bit rate occur (scaling of PLL); therefore, if the loss of lock signal ceases the selection or scaling of successive data rates also subsides)(column 16 lines 6-19 (scaling of PLL effects output transmission bit rate of serial data by changing ratio values Y and X)).

However, Johansen fails to disclose a functionally identical transmit circuit on the same integrated circuit as said receive circuit. Kato, from the same field of endeavor discloses an optical communication module (10, Fig 3) wherein the module contains both a signal reception process (110, Fig 3) and a signal transmission process (120, Fig 3) formed on a single integrated circuit semiconductor chip (abstract). At the time of invention, it would have been obvious to one of ordinary skill in the art to substantially duplicate the receive circuitry as taught by Johansen to create a transmit circuitry substantially similar to said receiver circuitry formed on a single integrated circuit semiconductor chip as taught by Kato. The motivation for having a pair of transmit/receive circuits would have been to create a bidirectional transponder module as opposed to a unidirectional transponder module. Also, having a module as taught by Kato allows for a loop-back path provided between the transmission IC and the reception IC to test for a correlation between input and output signals (Kato: page 1 paragraph 9). With further reference to claims 13 and 14, Johansen in view of Kato teach that the receiver having de-multiplexer (Johansen: column 3 lines 62-67 (receiver portion may comprise a de-multiplexer))(Kato: 131, Fig 2) and the transmitter having a multiplexer (Johansen: column 4 lines 1-6 (transmitting portion may comprise a multiplexer))(Kato: 151, Fig 2).

Furthermore, Johansen in view of Kato fail to disclose ceasing to adjust the selectable data rate once all selectable data rates have been attempted, whether or not the loss of lock signal has ceased. In applicants specification, applicant further defines the cessation of adjustment of the selectable data rate as in effect bypassing the CDR circuit (applicants specification: Figure 1305, 1406 (bypass, Figure 4))(applicants specification: 1614, Figure 5 (bypass))(applicants specification: page 20 paragraph 54 (CDR is designed to run at 4, 2, or 1 Gb/s or lower, if LOL

persists beyond these rates the CDR determines that the operational data rate is slower than 2 Gb/s and takes itself offline)).

Heston, from the same field of endeavor discloses an optical network element (204, Figure 2a), which selects from one of several selectable data rates (column 2 lines 29-30 (the present invention relates to a line card with multiple ports and multiple rates))(column 2 lines 55-60 (ports are configured to receive one of an OC-3, OC-12 or OC-48 signal))(column 7 lines 38-42 (clock and data recovery modules include mapping functionality which allows OC-3, OC-12 or OC-48 signals to be mapped to a common signal format)) and includes a controller that ceases to adjust the selectable data rate once all selectable data rates have been attempted (Figure 7 depicts at steps 708 and 712 attempts to adjust the selectable data rates until all selectable data rates, in this case, OC-3, OC-12 or OC-48 signals, have been attempted. Once all have been attempted data rate adjustment ceases)(column 7 lines 39-56 (if the incoming signal is not one of the selectable data rates (OC-3, OC-12 or OC-48 signals), for instance a Gigabit Ethernet signal, the signal bypasses the cdr module 312, in the same manner as the claimed invention)). Therefore, it would have been obvious to implement cessation of selectable data rate adjustment into the transponder system as taught by Johansen in view of Kato. The motivation for doing so would be to maximally utilize recovery circuitry for signals that are most common to telecommunications signaling and allows for use of less complicated and more conventional components (Heston: column 7 lines 48-56 (typical cdr modules allow programmable bandwidth limiting that provides the capacity to deliver OC-3, OC-12 or OC-48 signals and gigabit Ethernet services off the same physical ports which or coupled to optics)).

Response to Arguments

7. Applicant's arguments filed 3/2/07 with respect to claims 1-3 and 5-14 have been considered but are moot in view of the new ground(s) of rejection.

With respect to claims 9 and 12-13 applicant states that examiner only cited receiving portions of Johansen and did not identify transmit portions of Johansen which are configured to set the operational data rate of an optoelectronic device. However, the teachings of Johansen make it clear that operational data rates are set for both transmission and reception (column 1 lines 59-64 (the transponder system is capable of supporting transmission / reception of data streams at nominal bit rates including STM-1,4,16 and 64))(columns 1-2 lines 65-67 and 1-2 (transponder system supports both multi-rate reception and multi-rate reception))(column 5 lines 59-61 (outgoing data stream can be selected as nominal bit rate or transport bit rte independent of incoming data rate stream))(column 7 lines 45-65 (multi-rate selectable scaling applies to both the receiving part and transmitting part of the multi-rate transponder system))(column 8 lines 15-30 (transmitter scaling PLL locks onto incoming data streams at one or several bit rates))(column 8 lines 39-42 (outgoing data rate can be transmitted at same rate as incoming data rate))(column 16 lines 1-19)..

Applicant further states that the cited portions refer to a receiver chip rather than a transmit chip. Although cited portions do refer to receiver circuitry at some points, Johansen makes it clear in the description as well as the drawings that the transmission circuitry selects data rates in the same way as the receiver circuitry is explained to work (VCXO cited as providing the base for selectable data rates in first office action also operates as a VCO in the transmitter PLL loop (column 18 lines 13-14)). All of the components used to create a selectable

data rate in the receiver circuitry are also included in the transmit circuitry (Figure 3 includes clock generators 510 and 320, VCO 310 as well as selection of the transmitter scaling dividend using msel1...2).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth J. Malkowski whose telephone number is (571) 272-5505. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KJM 5/2/07

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER